

# Accellera Overview

April 21, 2017

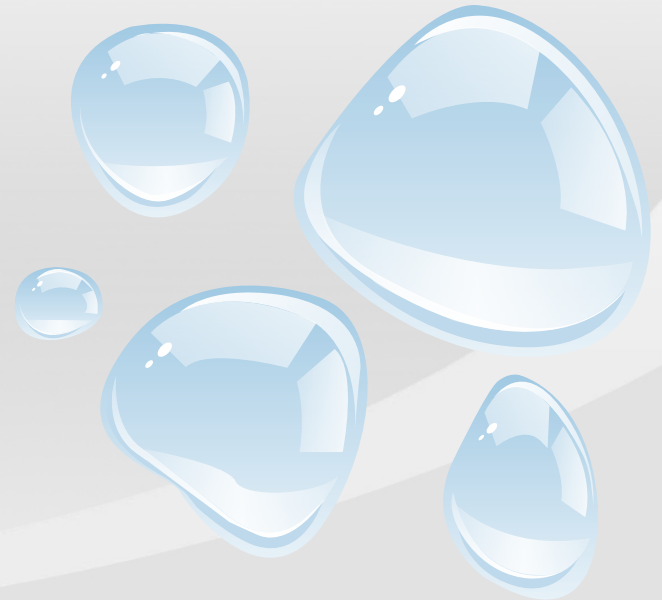
Dennis Brophy | Accellera Vice-Chairman



# Welcome

## Agenda

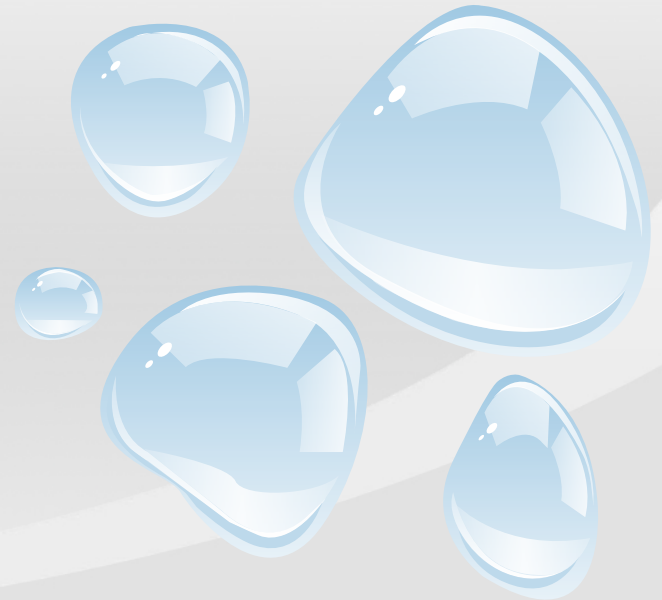
- About Accellera
- Current news
- Technical activities
- IEEE collaboration



# Accellera Systems Initiative

## Our Mission

To provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.



# Broad Industry Support

## Corporate Members

AMD

ARM

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# Broad Industry Support

## Associate Members

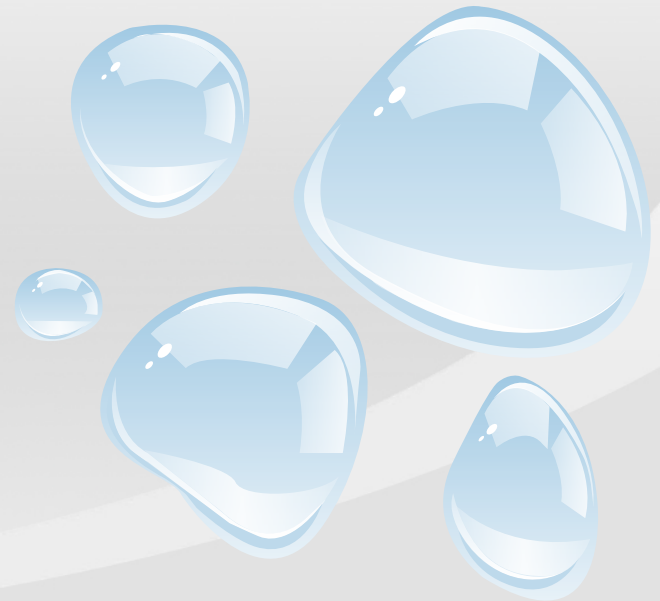


# Global Presence



## Agenda

- About Accellera
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# Accellera News

## ■ Standards

- IEEE Approves UVM 1.2 as IEEE 1800.2-2017
- Accellera relicenses SystemC reference implementation under Apache 2.0

## ■ Outreach

- First DVCon China to be held April 19, 2017
- Get IEEE free standards program extended 10 years/10 standards

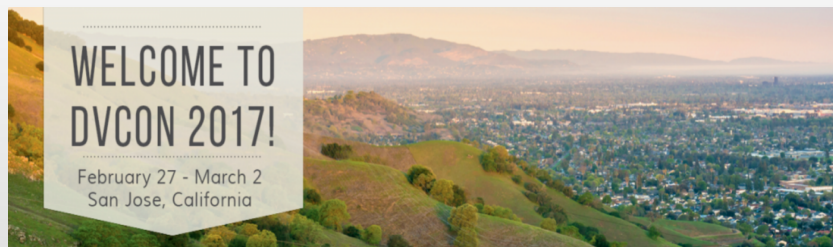
## ■ Awards

- Thomas Alsop receives 2017 Technical Excellence Award for his leadership of the UVM Working Group
- Shrenik Mehta receives 2016 Accellera Leadership Award for his role as Accellera chair from 2005-2010



# DVCon – Global Presence

## 29<sup>th</sup> Annual DVCon U.S.



[www.dvcon-us.org](http://www.dvcon-us.org)

## 4<sup>th</sup> Annual DVCon India



[www.dvcon-india.org](http://www.dvcon-india.org)

## 4<sup>th</sup> Annual DVCon Europe



[www.dvcon-europe.org](http://www.dvcon-europe.org)

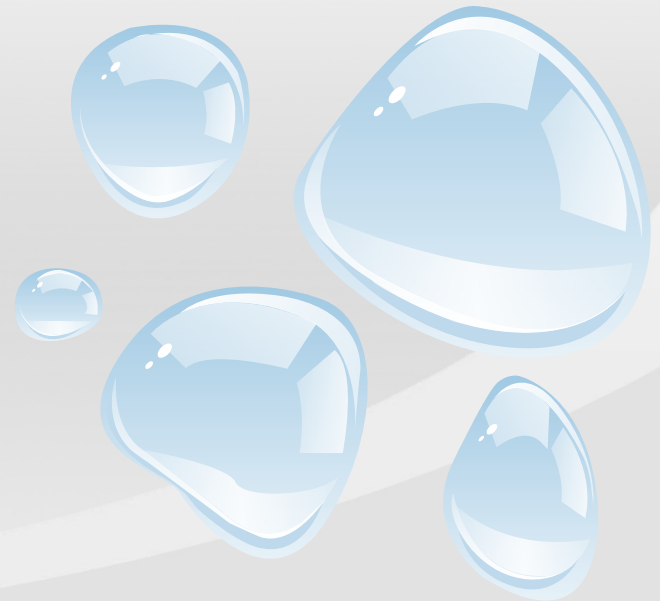
## 1<sup>st</sup> DVCon China



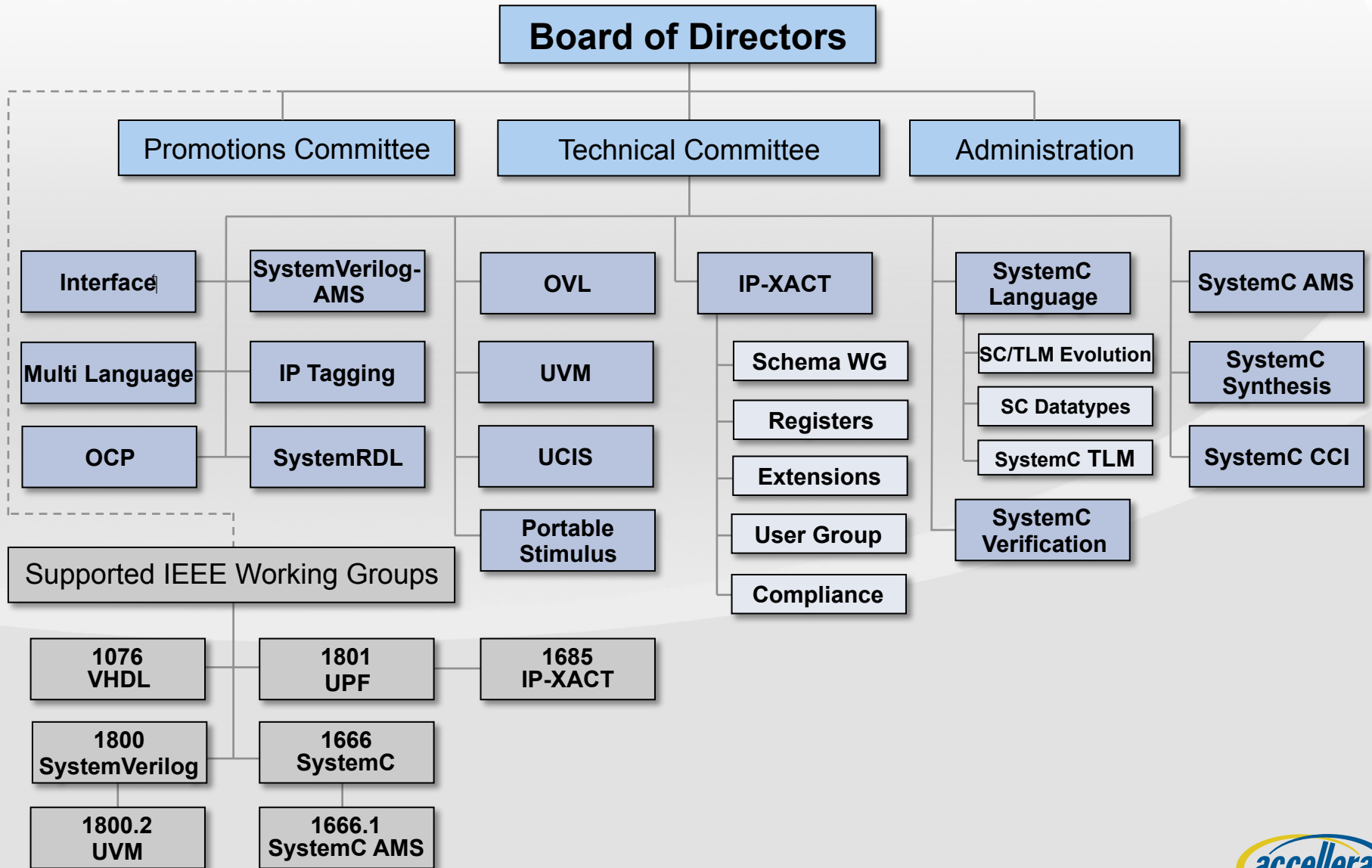
[www.dvcon-china.org](http://www.dvcon-china.org)

## Agenda

- About Accellera
- Current news
- **Technical activities**
- IEEE collaboration



# Accellera Systems Initiative



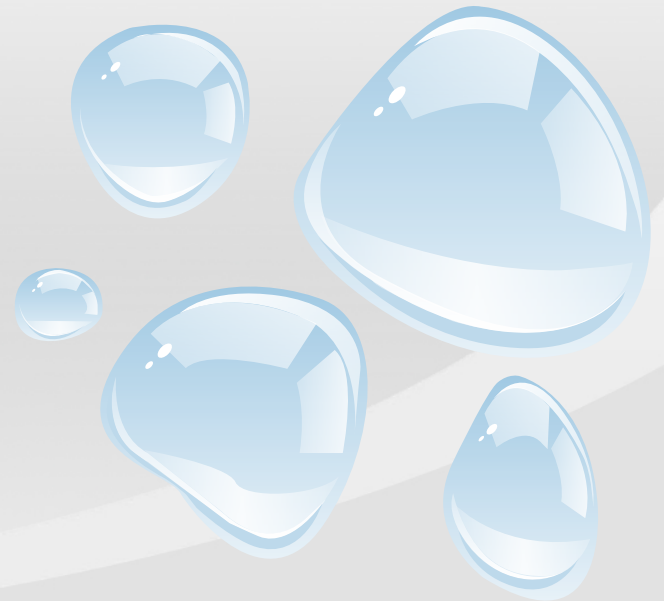
# Ongoing Technical Activities

## Current Standards and Activities

- Open Verification Library (OVL) 2.8.1
- Verilog-AMS (V-AMS) 2.4
- Standard Co-Emulation Modeling Interface (SCE-MI) 2.3
- Unified Coverage Interoperability Standard (UCIS) 1.0
- IP-XACT - Update of IEEE 1685 Issues and Vendor Extensions
- Intellectual Property (IP) Tagging 1.0
- Multi-Language (ongoing)
- Portable Stimulus (ongoing)
- SystemVerilog-AMS (ongoing)
- SystemC Synthesis 1.4.7
- SystemC Analog Mixed-Signal (AMS) 2.0
- SystemC LRM and Examples 2.3.1 (includes TLM 2.0)
- SystemRDL 1.0
- Open Source Companions:
  - UVM Reference Implementation 1.2
  - SystemC Proof of Concept Library 2.3.1
  - SystemC Verification Library (SCV) 2.0
  - UVM-SystemC 1.0-alpha version

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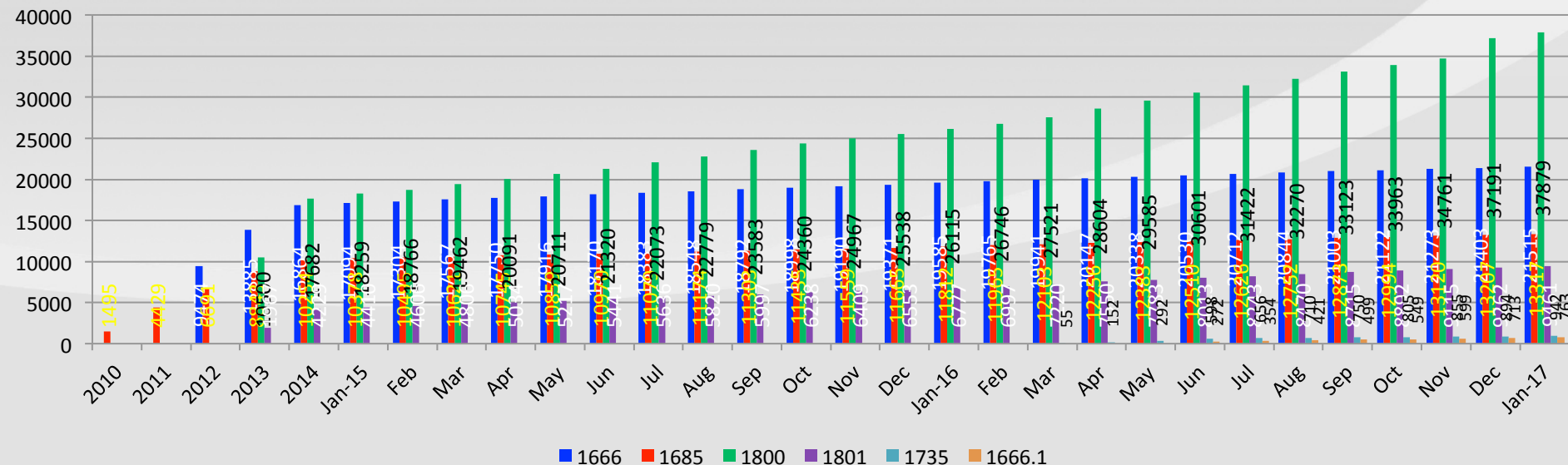
# Strong Partnership with IEEE

- IEEE Get program allows access to EDA & IP standards worldwide
- Download for free
  - 1666 SystemC
  - 1666.1 SystemC AMS
  - 1685 IP-XACT
  - 1800 SystemVerilog
  - 1800.2 UVM [coming soon!](#)
  - 1801 UPF
- Ongoing collaboration with the IEEE Standards Association
  - 1666 SystemC Language
  - 1666.1 SystemC Analog Mixed-Signal (AMS)
  - 1685 IP-XACT
  - 1800 SystemVerilog
  - 1800.2 Universal Verification Methodology (UVM)
  - 1801 Unified Power Format (UPF)
  - 1850 Property Specification Language (PSL)

# IEEE Standards Access at No Charge

- Accellera relationship with the IEEE-SA
- Accellera will release 10 standards for 10 years under an extended Get IEEE program
- More than **83,000 downloads** to date!

Cumulative Downloads 2010-2017



<http://standards.ieee.org/about/get/>

# Advancing Standards Together

- **Share your experiences**

- Visit [www.accelera.org](http://www.accelera.org) and register to post on forums at [forums.accelera.org](http://forums.accelera.org)

- **Show your support**

- Record your adoption of standards

- **Become an Accellera member**

- Join working groups



# THANK YOU

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